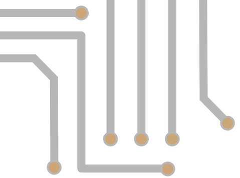


Latent Damage and Reliability in Semiconductor Devices

May1625 - Advisor & Client: Dr. Randy Geiger

Sean Santella Hayle Olson David Ackerman Jaehyuk Han

04/27/16

What is Latent Damage?

- ➔ Is usually caused by an Electrostatic Discharge (ESD) event
- ➔ Physically damages a device but is electrically undetectable

A device that has been *latently damaged* is still functional but may fail much sooner than expected.

Does Latent Damage exist?

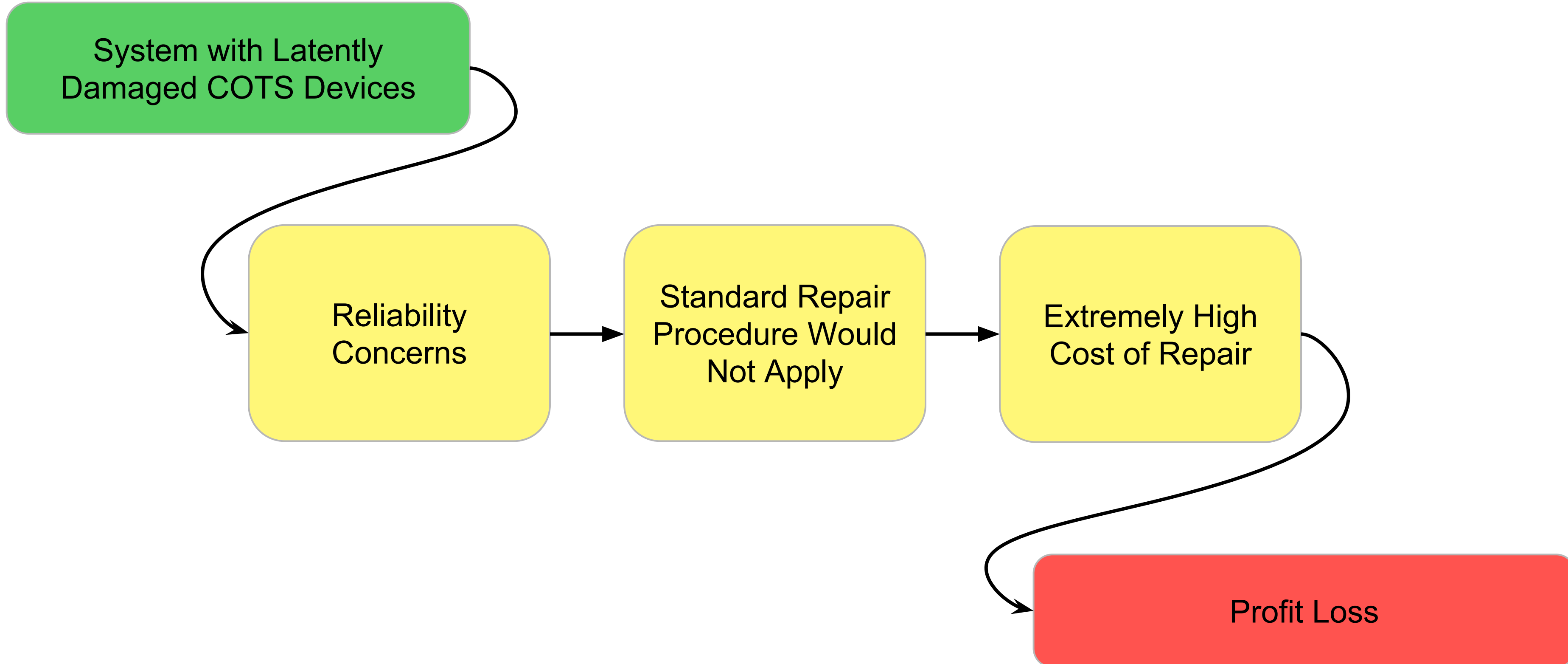
Some studies show that latent damage exists, while others don’t

- ➔ Latent damage is an on-going debate in the semiconductor industry

Study will examine bulk CMOS Commercial off-the-Shelf (COTS) devices

- ➔ COTS devices typically have a Mean Time to Failure (MTTF) of 20 years

Why should we care?



Hypothesis

If a non-catastrophic ESD event occurs on a semiconductor device, then latent damage exists.

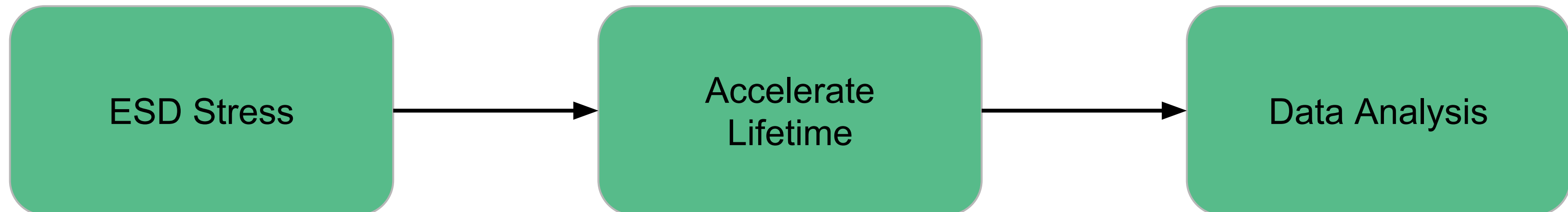
This latent damage can cause the reliability of these devices to decrease.

Resulting in the MTTF to be shorter than the manufacturing specifications.

Overall Project Plan

- ➔ Destroy 50% of our devices
  - ◆ Stress devices
- ➔ Accelerate the lifetime of the “functional” devices
  - ◆ Burn-in testing
- ➔ Observe and analyze the MTTF
  - ◆ Data analysis

An experiment with three parts:

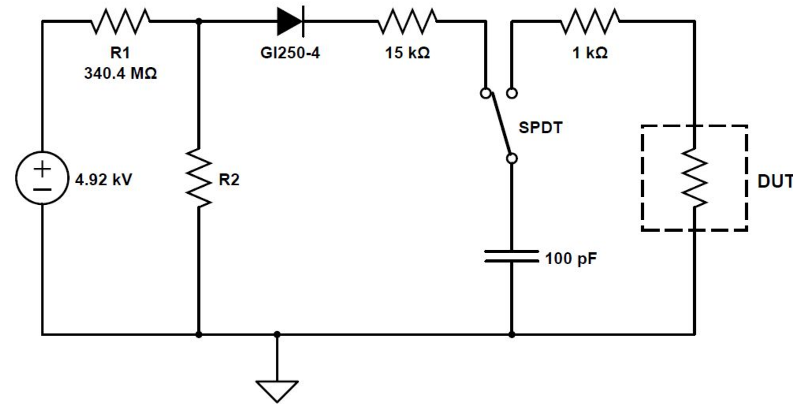


ESD Stress

ESD Stress

General Procedure

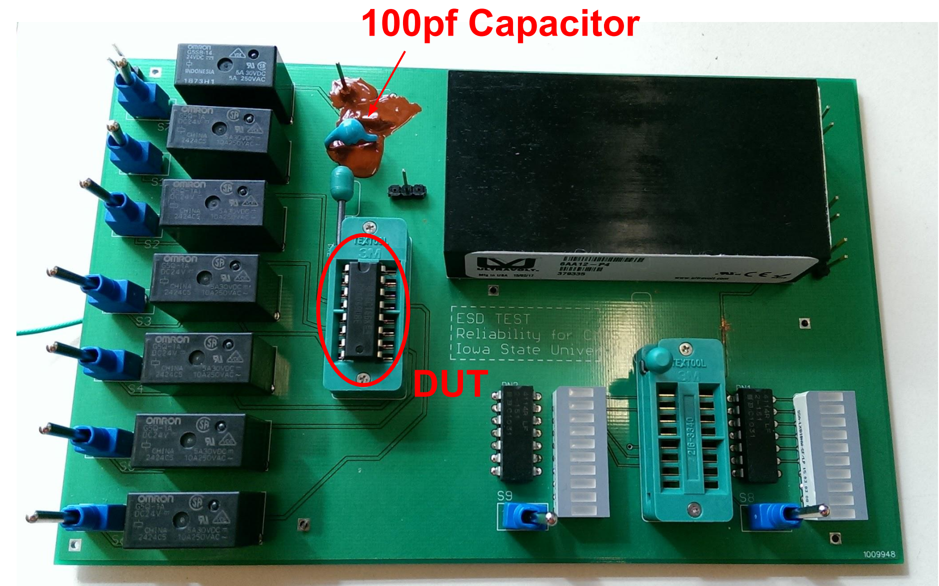
- Devices will be exposed to an ESD event at a high-voltage level
- Human Body Model (HBM)
  - 100pF Capacitor charged to a high-voltage
  - Discharged into Device Under-Test (DUT) with the output tied low
- Texas Instruments (CD4049UBE)
  - 6 CMOS inverters on one chip (hex inverter)
- Determine a maximum stress level



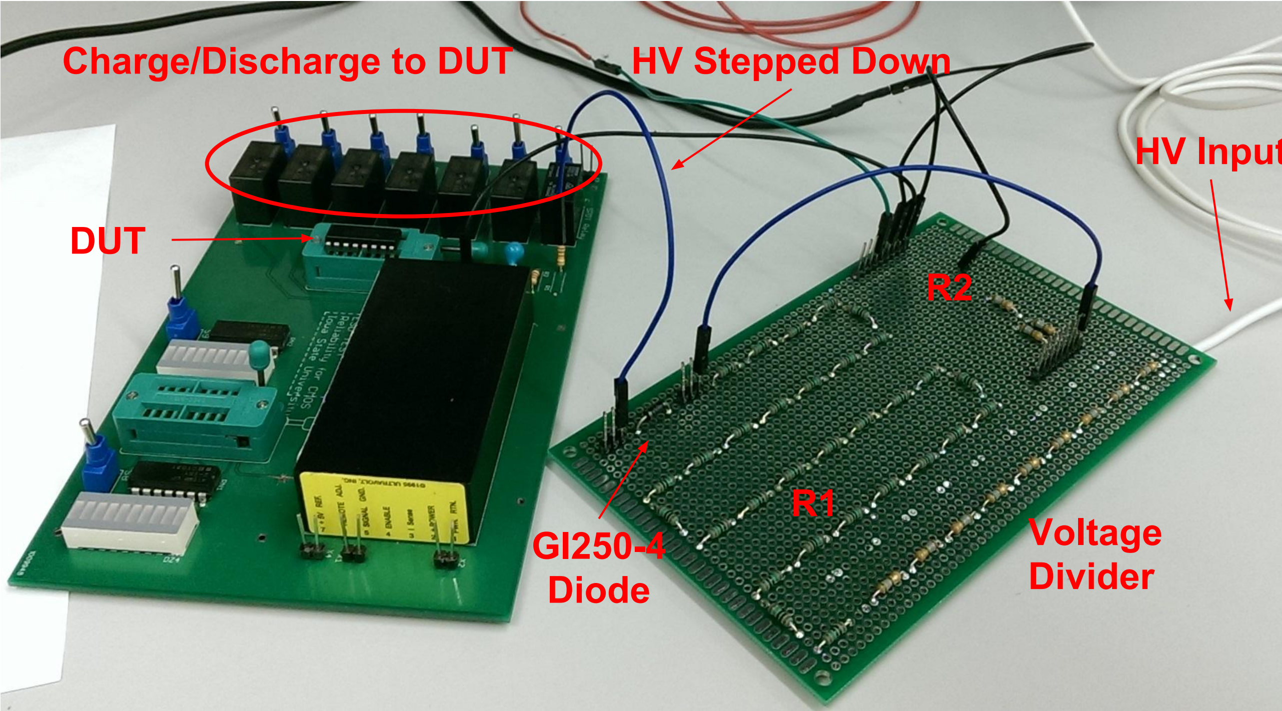
ESD Stress

PCB

- An ESD Stress PCB was previously created
  - Simulate an ESD event
  - Functionality check
- Programmable high-voltage source was non-functional
  - Re-purposed the PCB to use an agriculturally purposed high-voltage source



ESD Stress Setup

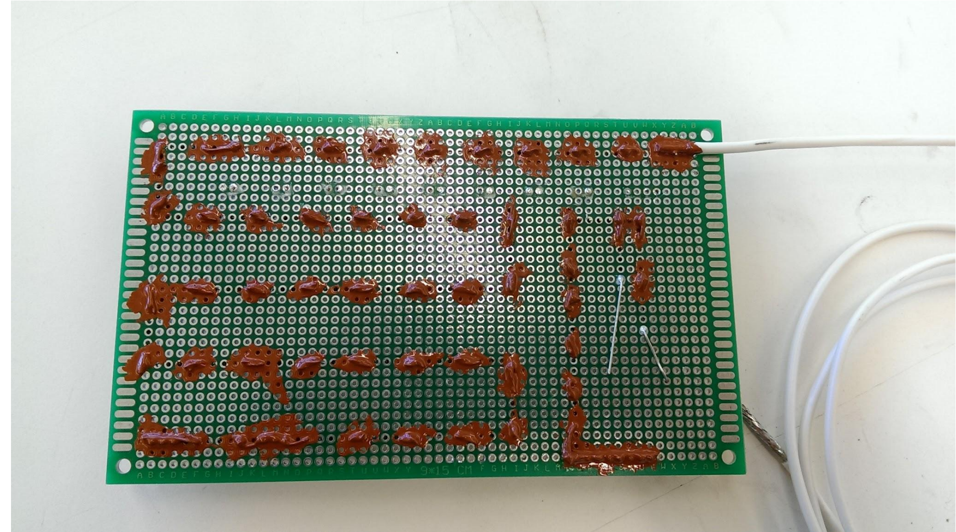


ESD Stress

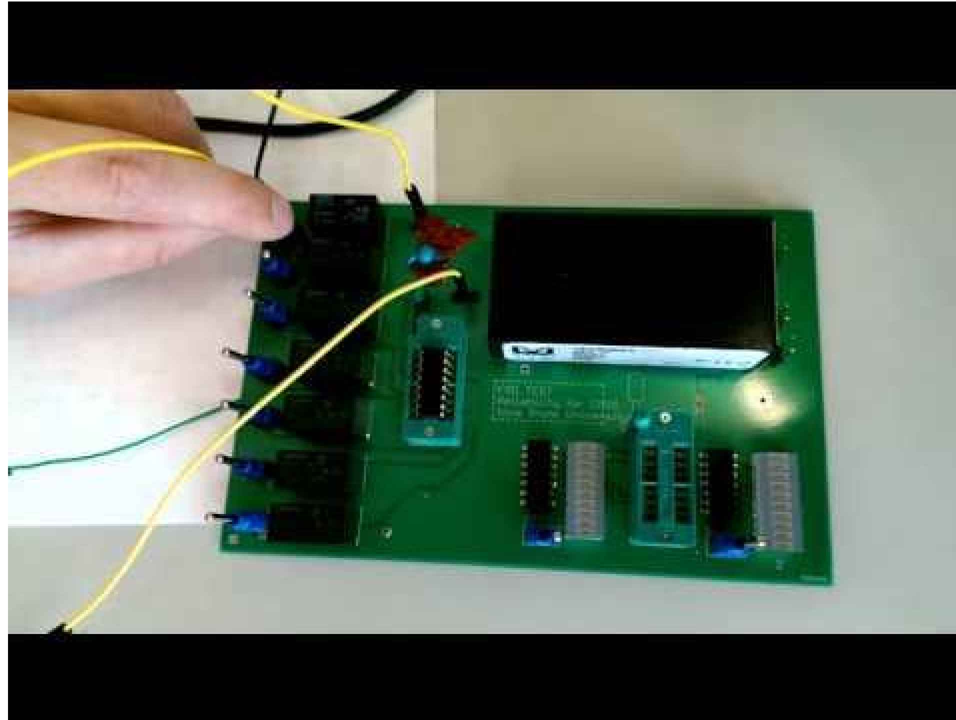
Challenges

- ➔ High-voltage source has high frequency content
  - ◆ High-speed diodes are required to minimize the effects
    - Typically do not have large reverse breakdown voltages (V_R)
- ➔ A high V_R is required to keep the capacitor charged during the negative cycle of the voltage source
  - ◆ A diode with a V_R of 4kV was used (Vishay SUPERECTIFIER GI250-4)
- ➔ Oscilloscope can only handle roughly 850V_{PP}
  - ◆ Designed and soldered an attenuator to check voltage on capacitor
- ➔ The only way to verify that the ESD Stress setup is working is to catastrophically damage a device with a high-voltage discharge
  - ◆ Components and devices used in the setup have to be soldered and insulated properly

Insulating Varnish

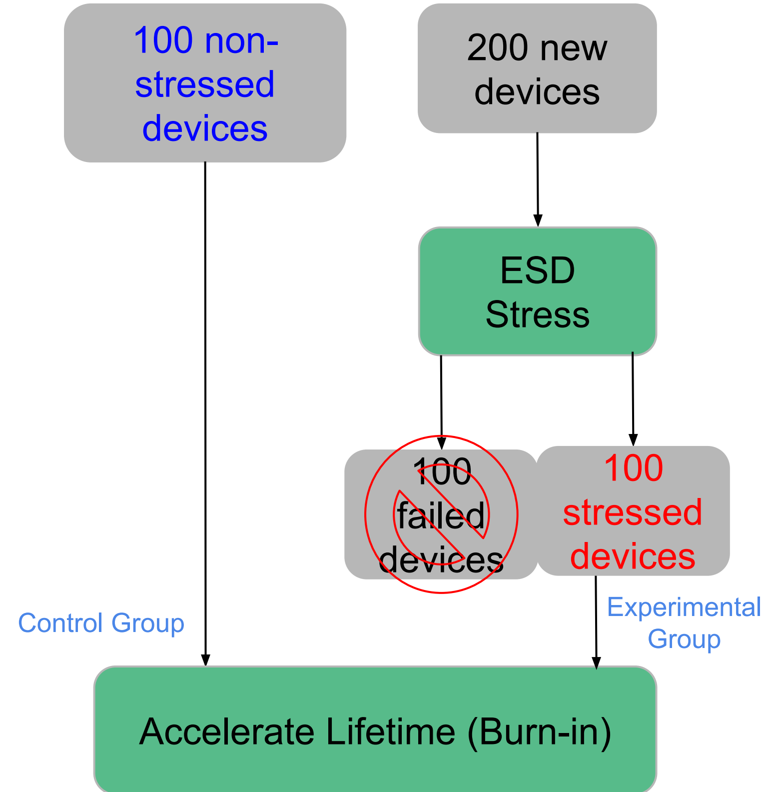


Stressing a Device



Test Samples

- ➔ Control Group
  - ◆ 100 non-stressed devices
  - ◆ 1 week of burn-in to acquire baseline data
- ➔ Experimental Group
  - ◆ 100 stressed devices
  - ◆ 1 week of burn-in



Lifetime Acceleration

Burn-in

General Procedure

Once the parts are stressed, they are put into a burn-in oven.

The burn-in oven is used to accelerate the lifetime of the devices.

- ➔ 112°C
  - ◆ MTTF acceleration: 20 years to 1 week
- ➔ DUTS are in a high-stress mode of operation

These parts will be checked regularly during the burn-in to determine if a failure has occurred.

Burn-in

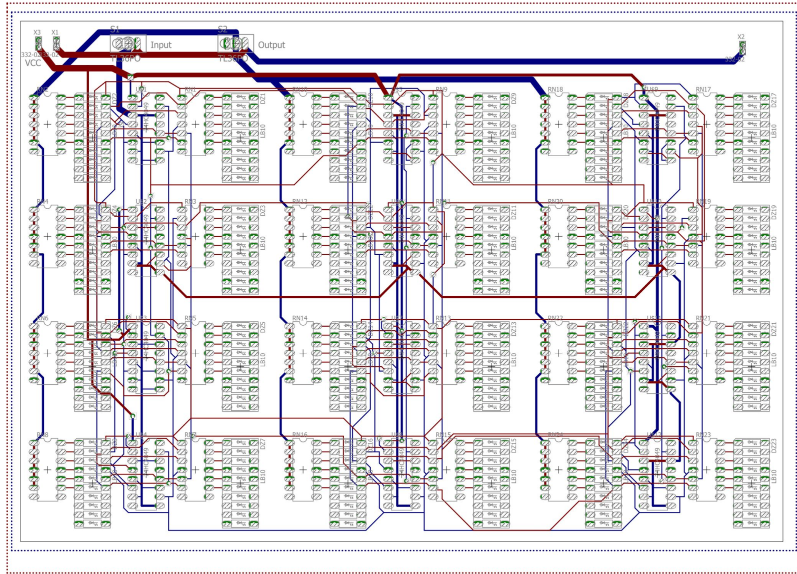
PCB

The PCB used to hold, test, and burn-in devices have two modes of operation:

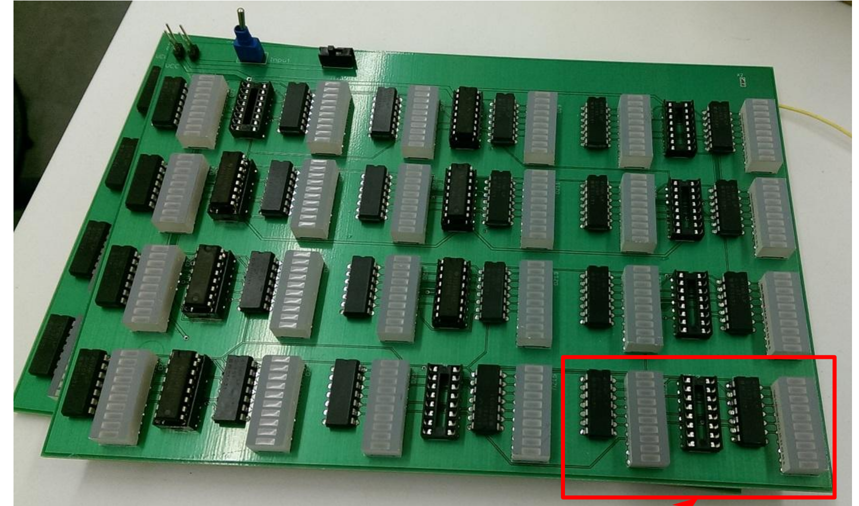
1. Further stress devices while in burn-in, by holding the output of DUTs at their trip point.
2. Test the digital logic functionality of the devices, by disconnecting the output of the DUTs, to check when the devices failed.

Burn-in PCB

1st Design

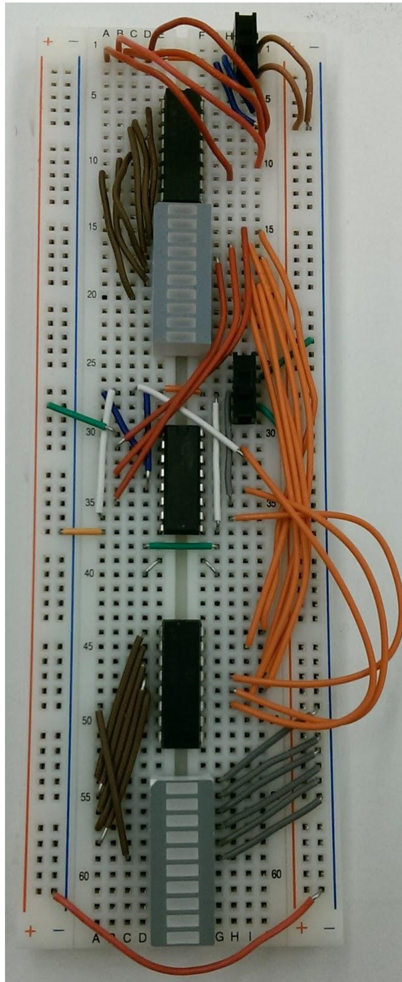


12 Testing Clusters per PCB



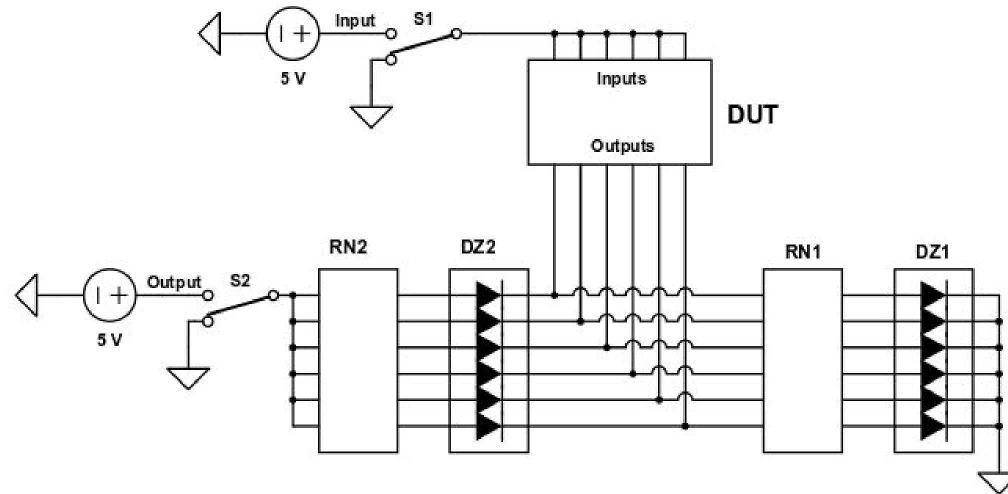
1 Testing Cluster

Burn-in PCB



1st Design

- ➔ The bread board on the left is to test a *single* hex-inverter
- ➔ Circuit schematic:



Burn-in PCB

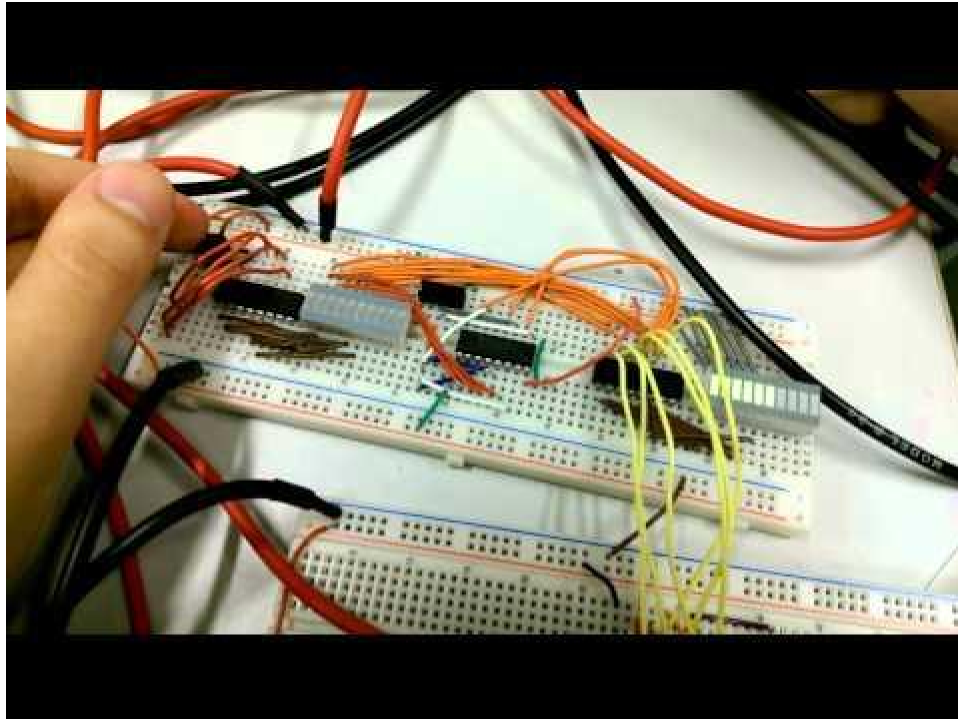
Functionality Check

In the table below, 1 means “high” for the switch states, and 1 means conducting for the components.

Switch		Diodes		Inverter Transistors	
“Input”	“Output”	DZ1	DZ2	PMOS	NMOS
0	0	1	0	1	0
0	1	1	0	1	0
1	0	0	0	0	1
1	1	0	1	0	1

Burn-in PCB

Functionality Check



Burn-in PCB

1st Design - Issues

1. Resistor networks in the testing set-up are bussed instead of isolated.

2. All output gates of each testing setup are connected with other output gates

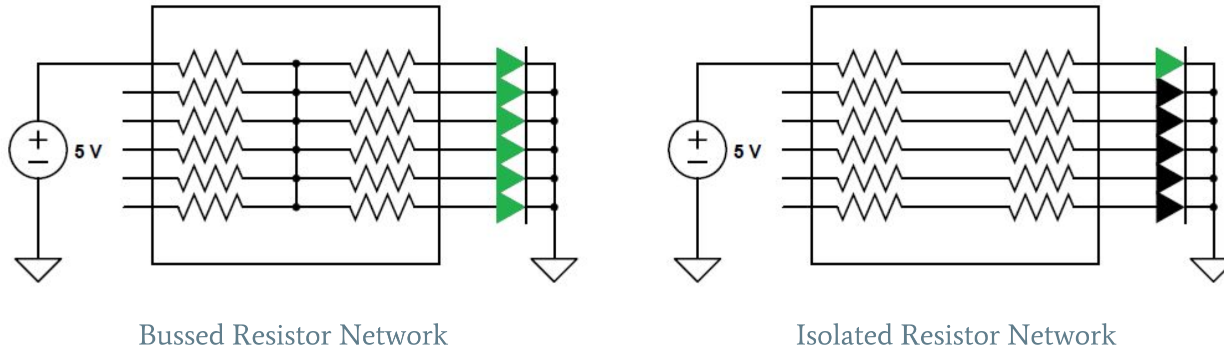
These are design flaws that broke functionality of the old boards.

We chose to make new boards to solve these issues.

Burn-in PCB

1st Design - Issues

1. Resistor networks in the testing set-up are bussed instead of isolated.



Bussed Resistor Network

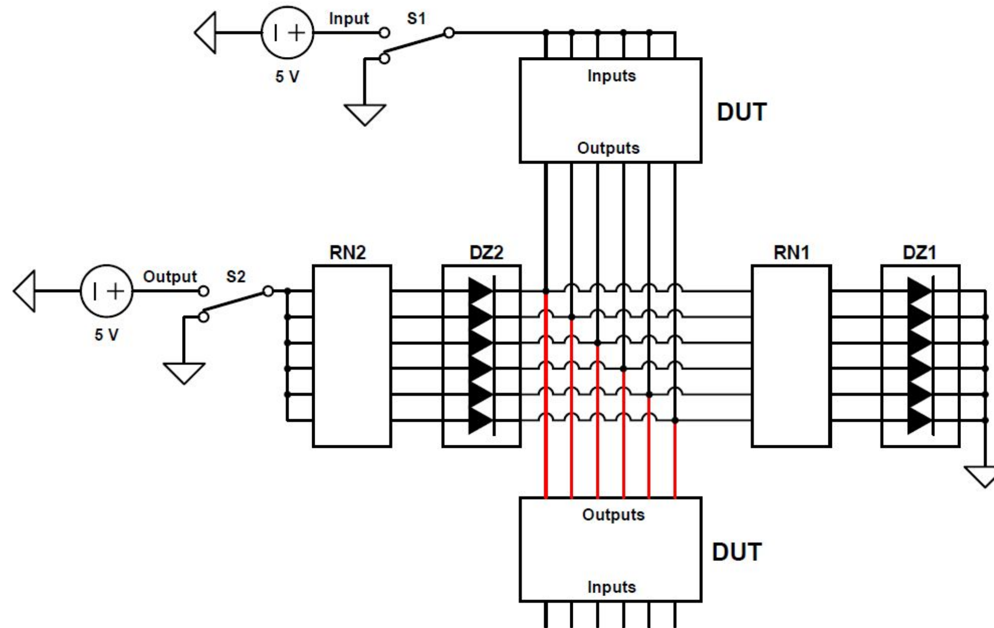
Isolated Resistor Network

The LEDs are the visual indicators for collecting burn-in data; they need to work accurately

Burn-in PCB

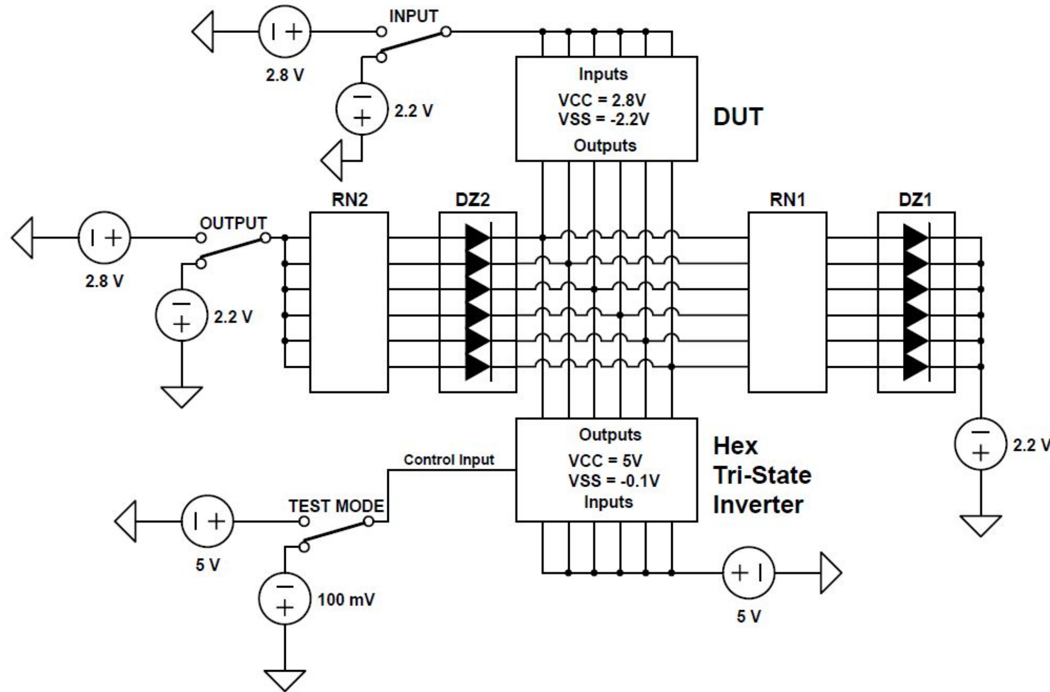
1st Design - Issues

2. Output gates of each testing setup are connected with other output gates



Burn-in PCB

2nd Design

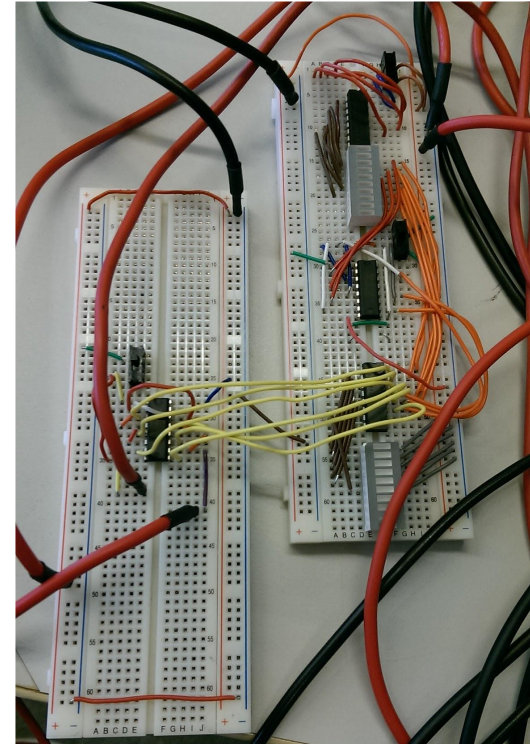


- New circuitry to allow electronic switching of operation modes
    - Output of DUT is either at the trip point or floating (disconnected) relative to the tri-states

Burn-in PCB

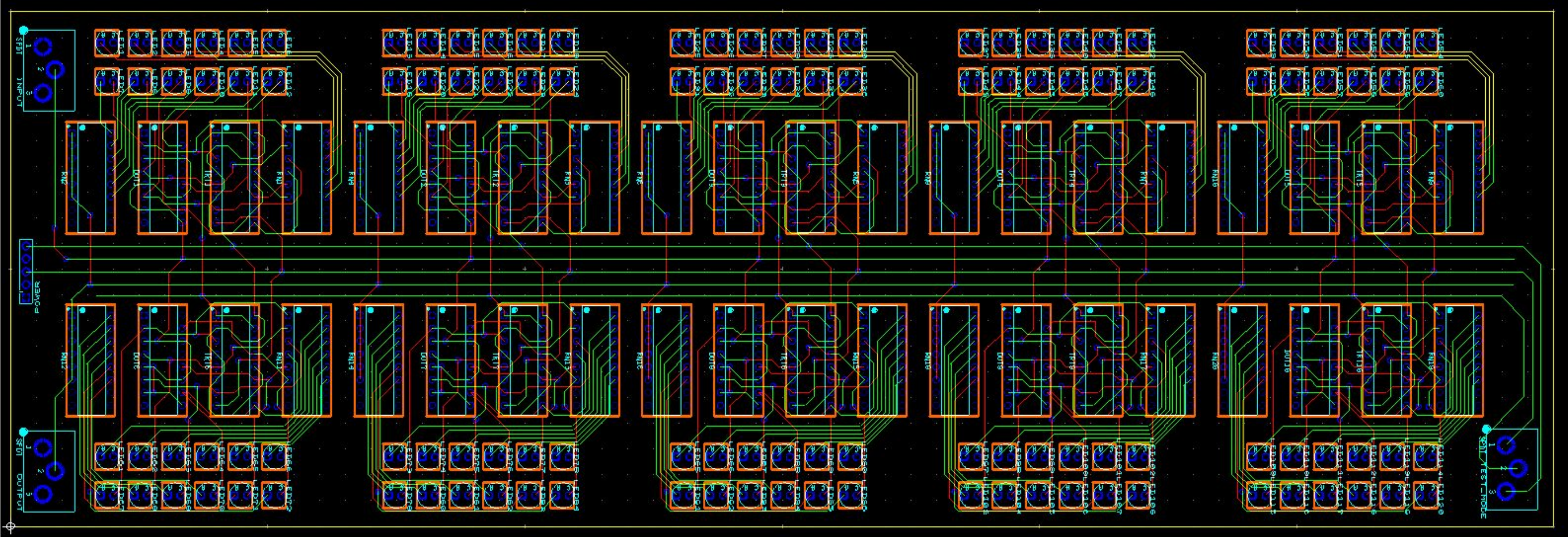
2nd Design

- ➔ Without the new circuitry, we would need 600 extra switches for the population.
- ➔ Use of the tri-states only requires one extra switch per board, compared to the 1st design.



Burn-in PCB

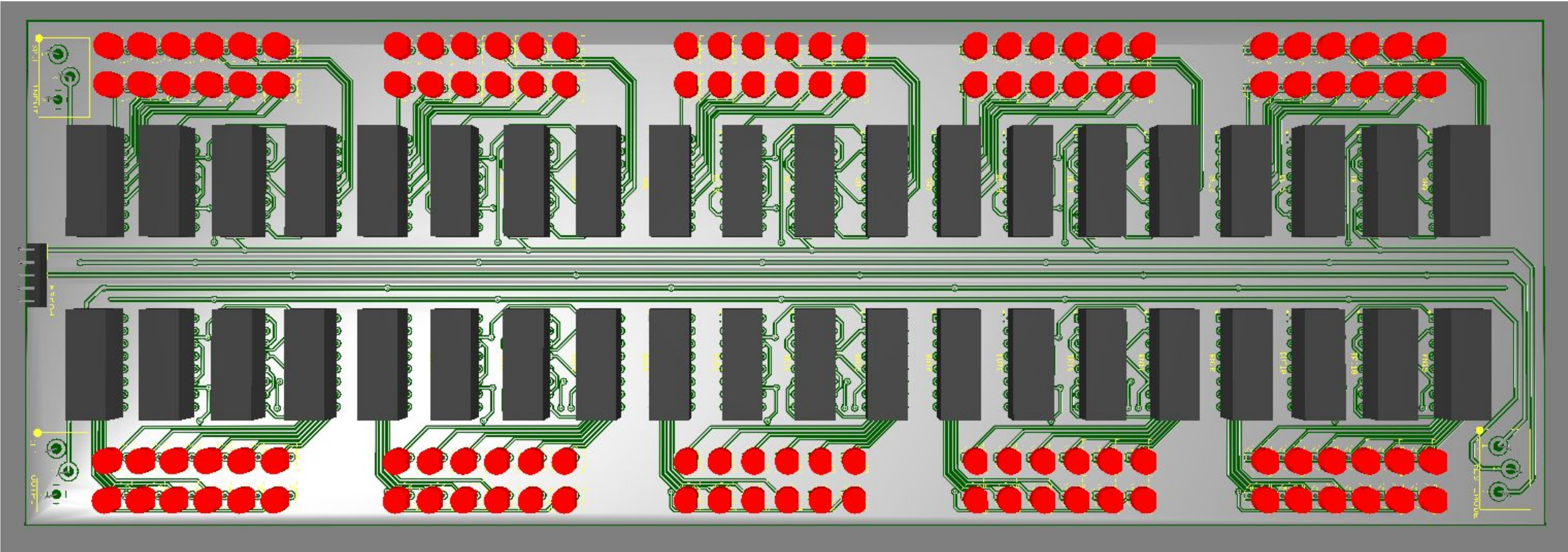
2nd Design



10 Testing Clusters per PCB

Burn-in PCB

2nd Design



Burn-in PCB

2nd Design

- ➔ Components need to withstand a temperature of 112°C
- ➔ With the current design, these do not meet the specification:
  - ◆ SPST Slide Switch [GF-123-0054]
  - ◆ LED 3mm [OVLBR4C7]
- ➔ The headers are okay because we can remove the plastic

Component	Temp
PCB (FR-4)	140°C
Socket	125°C
Hex Buffer	125°C
Tri-St. Inverter	125°C
Resistor Array	125°C
Switch	104°C
LED 3mm	100°C
Headers (UL94V-0)	90°C

Reaching our Current Design

- Determined issues with the 1st design of the burn-in PCB
  - Resistor networks bussed
  - DUT output gates connected
- Solved the burn-in temperature with the HTOL model (112°C)
- Redesigned the burn-in PCB with electronic switching circuitry
  - Hex tri-state inverters
- Diagnosed some issues with the ESD stress PCB
  - Insulating varnish to eliminate arcing
- Considered our safety as a great concern
  - Insulating varnish, properly insulated wires, soldering high-voltage circuits rather than breadboarding, etc.

Data Analysis

Data Analysis

General Procedure

After collecting the burn-in data for the experimental group, we can compare this to the control group data.

This will require statistical analysis, however our conclusion will only be accurate to a certain confidence level.

Our primary statistic of interest will be the *difference* in MTTF between the experimental and the control group.

Completed Work

- ➔ Replaced the programmable high-voltage source
- ➔ Determined issues and intended operation of existing PCB's
- ➔ Breadboard implementation of 1st burn-in PCB design
- ➔ Added second functionality to burn-in PCB
  - ◆ High-stress mode
- ➔ Calculated the burn-in temperature (112°C)
- ➔ Created 2nd burn-in PCB design
- ➔ Attempted to stress devices while troubleshooting high-voltage source

Future Considerations

- Establish maximum stress level with ESD Stress System
- Stress devices to create Experimental Group
- Replace burn-in PCB components
  - Must be rated at 112°C
- Fabricate 10 burn-in PCBs and order components
- Populate and solder burn-in PCB components
- Accelerate lifetime of devices (burn-in)
  - Control Group
  - Experimental Group
- Record data during burn-in of individual failing inverters
- Analyze data to either confirm or deny hypothesis
  - Only to a certain degree of confidence

Thank you!

Any Questions?

Project Milestones & Schedule

	Task Name	Start Date	End Date	% Complete
1				
2		08/24/15	04/29/16	
3	Fall 2015 Semester	08/24/15	09/01/15	50%
4	Project Assignments	08/24/15	09/01/15	100%
5	Research	09/01/15	10/07/15	100%
6	Website	09/16/15	09/30/15	100%
7	Project Plan V1	09/30/15	10/02/15	100%
8	Order Parts	10/07/15	10/19/15	100%
9	Design Document V1	10/20/15	10/23/15	100%
10	Prepare Presentation	11/10/15	12/08/15	100%
11	Presentation of Implementation	12/08/15	12/08/15	100%
12	Spring 2016 Semester			
13	Design & Verify Test System	01/11/16	04/11/16	
14	Burn-in PCB			90%
15	ESD Stress PCB			95%
16	Fabricate Burn-in PCB's	04/11/16	04/18/16	0%
17	Populate Burn-in PCB's	04/18/16	04/25/16	0%
18	Burn-in Devices for 1 week	04/25/16	05/02/16	0%
19	Data Analysis	05/02/16	05/03/16	0%
20	Verify Hypothesis	05/03/16	05/03/16	0%
21	Prepare Presentation	03/28/16	04/29/16	90%
22	Final Presentation	04/27/16	04/29/16	

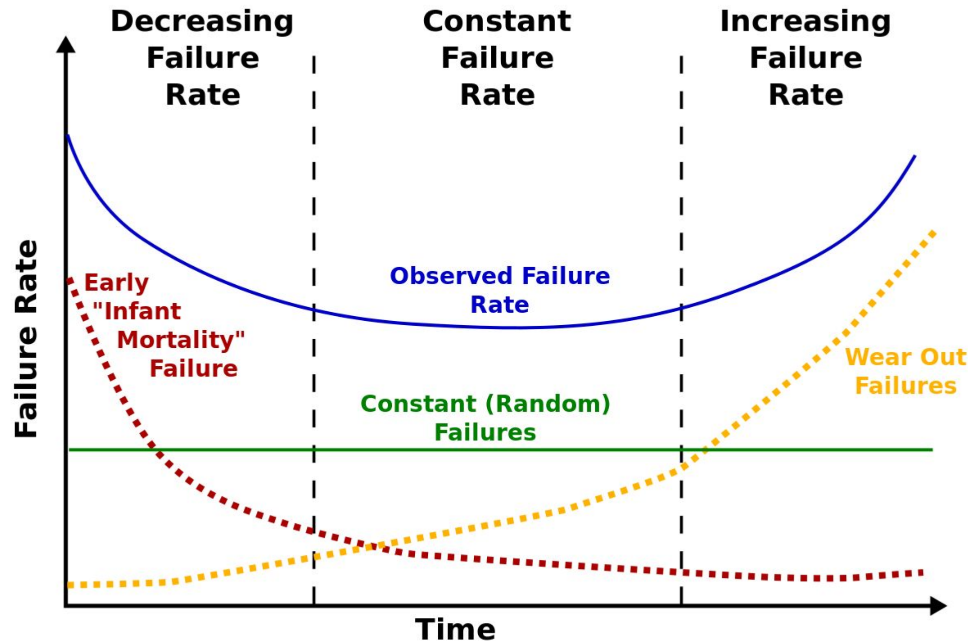
Updated on April 5th, 2016

Resource/Cost Estimate

Bill of Materials - May1625						Updated: April 12th 2016
Item	**Qty.**	**Reference**	**Cost**	**Part Description**	**Supplier**	**Supplier #**
1	10	Murata Cermic Disc Capacitors 100pf	-	DHRB34A101M2BB	Mouser	81-DHRB34A101M2BB
2	2	1st Design ESD Stress PCB	-	Provided	-	-
3	10	1st Design Burn-in PCB	-	Provided	-	-
4	1	Electric Fencer High-Voltage Source	$53.49	5kV 0.2J	Gallagher	M20
5	1	Digital Electric Fence Tester	$36.37	Tests up to 20kV 3 Digit Read Out	Zareba	DEFT-Z
6	50	10M Resistors (.25W)	$5.74	RNV14FAL10M0	Digi-Key	RNV14FAL10M0CT-ND
7	1	MG Chemicals Insulating Varnish	$9.44	Red GLPT 55ml Bottle	Amazon	4228-55ML
8	10	Texas Instruments Tri-St. Inverters (Hex)	$5.81	CD74HC366E	Digi-Key	296-33070-5-ND
9	20	Vishay Diode 4kV 250mA	$7.08	GI250-4-E3/54	Digi-Key	GI250-4-E3/54GICT-ND
		TOTAL COST	$117.93			

Semiconductor Reliability

Bathtub Curve



Source: www.en.wikipedia.org/wiki/Bathtub_curve

Burn-in

Calculations - HTOL Model

Variables:

A_f: acceleration factor
k: Boltzmann's Constant
E_a: activation energy (eV)
T: temperature (Kelvin)

D: number of devices tested (100 devices)
H: test hours per device (168 hours = 1 week)
EDH: equivalent device hours
r: number of failures (50 fails)

Failures in Time (FIT) to Mean Time to Failure (MTTF):

$FIT = \lambda_{FIT} = \lambda_{hours} \times 10^9$ (Failure rate (λ) per billion hours)

$MTTF_{hours} = 1/\lambda_{hours}$ (Mean Time to Failure)

Source: www.microsemi.com

Burn-in

Calculations - HTOL Model

$MTTF_{years} = 20$

$MTTF_{hours} = 8760 \times MTTF_{years} = 8760 \times (20)$ ⇒ $MTTF_{hours} = 175{,}200$

$\lambda_{hours} = 1/MTTF_{hours} = 1/(175{,}200)$ ⇒ $\lambda_{hours} = 5.708 \times 10^{-6}$ fails/hour

$EDH = r/\lambda_{hours} = (50 \text{ fails})/(5.708 \times 10^{-6} \text{ fails/hour})$ ⇒ $EDH = 8{,}760{,}000$ hours

$A_f = EDH/(D \times H) = (8{,}760{,}000 \text{ hours})/(100 \times 168 \text{ hours})$ ⇒ $A_f = 521.43$

Solve for T_{test} to determine burn-in temperature:

$$A_f = e^{\left[\left(\frac{E_a}{k}\right)\left(\frac{1}{T_{use}}-\frac{1}{T_{test}}\right)\right]} = 521.43 = e^{\left[\left(\frac{1.2eV}{8.617*10^{-5}\frac{eV}{K}}\right)\left(\frac{1}{328K}-\frac{1}{T_{test}}\right)\right]}$$

⇒ **$T_{test} = 384.69K \approx 112°C$**